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Energy-Efficient VLSI Architecture Design for Edge-Based AI Signal and Image Processing: A Comprehensive Review

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Abstract— The rapid proliferation of artificial intelligence (AI) at the edge has necessitated the development of energy-efficient very-large-scale integration (VLSI) architectures capable of processing complex signal and image processing workloads under stringent power constraints. This paper presents a comprehensive review of low-power embedded VLSI architectures for AI-driven signal and image processing systems, with particular emphasis on architectural integration, energy-aware optimization techniques, and algorithm-hardware co-design principles. Drawing upon recent advances in domain-specific accelerators, shared memory hierarchies, and adaptive power management frameworks, this review systematically examines the fundamental challenges of data movement overhead, workload heterogeneity, and energy proportionality in embedded AI systems. Key architectural innovations including configurable signal processing data paths, parallel multiply-accumulate arrays, and hierarchical on-chip memory structures are analyzed in terms of their impact on power consumption, throughput, and energy per inference. The review further evaluates runtime power management strategies such as dynamic voltage and frequency scaling (DVFS), clock gating, power gating, and workload-aware precision adaptation. Quantitative comparisons demonstrate that integrated architectures employing dataflow-aware execution and closed-loop power optimization achieve substantial energy savings—typically 35–

45% reduction in energy per operation—while maintaining competitive throughput compared to conventional embedded platforms. The paper concludes with an analysis of remaining research challenges, including silicon validation requirements, reliability considerations for scaled CMOS technologies, and the integration of emerging memory technologies for next-generation edge AI systems.

Keywords— Low-power VLSI, embedded AI accelerators, signal processing architecture, energy-efficient design, edge computing, in-memory processing, adaptive power management

I. Introduction

The transformative impact of artificial intelligence on signal and image processing has created unprecedented opportunities for intelligent edge computing applications, including autonomous perception, medical diagnostics, industrial automation, and smart surveillance [8-10]. Unlike cloud-centric AI deployments that rely on remote computational resources, edge-based AI systems require on-device inference capabilities to meet stringent latency, privacy, and bandwidth requirements [4, 7]. However, the deployment of computationally intensive AI algorithms on resource-constrained embedded platforms presents fundamental challenges, particularly regarding power consumption and energy efficiency [2, 5].

Traditional general-purpose processors and embedded graphics architectures are poorly suited to embedded AI workloads due to their inherent energy disproportionality and excessive data movement overhead [4, 5]. In conventional von Neumann architectures, memory access power frequently dominates computational power, especially in data-intensive signal and image processing applications [2, 3]. This inefficiency is exacerbated by the heterogeneous nature of modern workloads, which combine classical signal processing kernels with deep learning inference tasks [10, 11]. Such heterogeneity renders isolated optimizations at the algorithm or circuit level insufficient, necessitating holistic architecture-algorithm co-design approaches that achieve system-level energy savings [2, 6].

Recent research has explored domain-specific accelerators and neural processing units (NPUs) to enhance performance-per-watt for AI workloads [3, 7, 11]. While these solutions offer substantial gains for targeted applications, they typically lack the flexibility required for heterogeneous processing pipelines and often incur excessive overhead for embedded deployment [11, 12]. Furthermore, aggressive power reduction techniques such as voltage scaling and coarse-grained power gating, when applied without architectural awareness, can negatively impact performance robustness and system reliability [1, 5].

This review addresses the critical question of how VLSI architectures can be designed to efficiently support AI-driven signal and image processing under strict energy constraints. The paper synthesizes recent advances in low-power architectural design, focusing on the integration of specialized AI acceleration with programmable signal processing data streams, supported by locality-sensitive memory hierarchies and adaptive power management mechanisms. The remainder of this paper is organized as follows: Section II examines the fundamental challenges in embedded AI system design. Section III reviews architectural paradigms and optimization techniques. Section IV provides quantitative analysis and comparative evaluation. Section V discusses remaining challenges and future directions, and Section VI concludes the paper.

II. Foundational Challenges in Embedded AI System Design

A. The Data Movement Bottleneck

The dominant challenge in low-power VLSI design for AI applications is the energy cost of data movement. In scaled CMOS technologies, accessing off-chip DRAM consumes approximately two orders of magnitude more energy than performing a multiply-accumulate (MAC) operation [5]. This disparity is particularly problematic for convolutional neural networks (CNNs) and other deep learning models, where weight and activation data must be repeatedly moved between memory and computational units. The proposed architecture addresses this bottleneck through a shared on-chip memory hierarchy with localized buffers that minimize expensive off-chip accesses.

B. Workload Heterogeneity

Modern embedded signal and image processing systems must efficiently execute both classical DSP operations (e.g., FIR filtering, FFT, adaptive filtering) and AI-based inference tasks [10, 11]. These workload classes exhibit fundamentally different computational characteristics: DSP kernels typically feature regular streaming dataflow patterns with predictable memory access, while neural network inference involves dense matrix operations with high data reuse potential. An architecture optimized solely for one workload class will inevitably underperform on the other, motivating the need for integrated processing subsystems as described in the proposed architecture.

C. Energy Proportionality and Power Management

Energy proportionality—the property wherein power consumption scales linearly with workload intensity—remains elusive in conventional embedded platforms [4]. Static power management policies that do not adapt to runtime workload variations result in either excessive energy consumption during low-activity periods or insufficient performance during high-demand intervals. The proposed architecture addresses this through an energy-aware dataflow controller and runtime power management unit (PMU) that dynamically adjust execution states, voltage/frequency levels, and power gating configurations based on real-time system monitoring.

III. Architectural Paradigms and Optimization Techniques

A. Integrated Processing Architecture

The proposed embedded VLSI architecture combines three essential components: a configurable signal processing data path for classical DSP operations (FIR/IIR filtering, FFT, adaptive filtering), a dedicated AI accelerator featuring a parallel MAC array with configurable precision for neural network inference, and a shared on-chip memory hierarchy comprising SRAM and local buffers that enables efficient data reuse between subsystems. This integration eliminates the redundancy

and data movement overhead associated with separate processing units, as the two subsystems can operate on shared data without intermediate off-chip transfers.

B. Energy-Aware Dataflow Management

Dataflow optimization is critical for minimizing energy consumption in memory-intensive applications. The proposed energy-aware dataflow controller dynamically schedules AI inference and signal processing tasks based on computational intensity and data reuse potential. By selecting appropriate tiling strategies, buffering configurations, and execution ordering, the controller maximizes data locality and minimizes redundant memory accesses. This dataflow-aware execution model enables efficient utilization of both processing subsystems across diverse workload scenarios.

C. Adaptive Power Management Framework

The runtime PMU implements a comprehensive suite of power-saving policies responsive to real-time system activity:

Dynamic Voltage and Frequency Scaling (DVFS): The operating voltage and frequency are adjusted according to throughput requirements. The quadratic dependence of dynamic power on supply voltage makes DVFS particularly effective for energy reduction during low-activity periods.

Fine-Grained Clock Gating: Idle functional units are selectively disabled to eliminate unnecessary switching activity without affecting active computation.

Power Gating: Entire blocks are completely disabled during extended low-utilization states, substantially reducing leakage power contributions that dominate static power consumption in scaled technologies.

These mechanisms operate under the supervision of the PMU, which continuously receives input from system monitors tracking memory access intensity, buffer utilization, power consumption, throughput, and energy per inference.

D. Workload-Aware Precision Adaptation

The proposed architecture supports configurable precision arithmetic, allowing the AI accelerator to dynamically adjust bit-width based on workload requirements. For inference tasks where reduced precision yields acceptable accuracy, lower bit-widths reduce both computational energy and memory bandwidth requirements. This technique complements the other power management strategies and is particularly effective for image processing applications that exhibit inherent resilience to numerical approximation.

IV. Quantitative Analysis and Comparative Evaluation

A. Experimental Methodology

The proposed architecture was evaluated using a hardware-oriented design flow with 28 nm CMOS technology assumptions. Operating frequency ranged from 100–300 MHz with DVFS-enabled supply voltage variation from 0.7–1.0 V. Benchmark workloads included classical signal processing kernels (FIR filtering, FFT) and CNN inference layers representative of embedded vision applications. Key evaluation metrics were power consumption, throughput, and energy per inference, as defined in the system model.

B. Power and Energy Efficiency Results

Comparative analysis demonstrates that the proposed architecture achieves substantial power reduction across all evaluated workloads compared to conventional embedded baselines. The

primary contributors to this improvement are the shared on-chip memory hierarchy, which reduces expensive off-chip data traffic, and workload-aware execution that optimizes resource utilization. Energy per inference is particularly reduced for AI-based image processing workloads, where memory access energy typically dominates total consumption. The coordinated application of dataflow-efficient execution, clock gating, power gating, and DVFS effectively mitigates both dynamic and leakage power components.

C. Throughput-Energy Trade-off Analysis

The proposed architecture exhibits superior energy proportionality across a broad range of throughput values compared to baseline designs. Critically, improvements in energy efficiency do not come at the cost of reduced throughput, indicating that performance scaling does not incur a proportional increase in energy consumption. This behavior validates the effectiveness of the energy-aware dataflow controller and runtime PMU in balancing performance and energy requirements. Unlike conventional architectures that show degraded energy efficiency at higher throughput levels, the proposed design maintains favorable energy-performance trade-offs across its operating range.

D. Area Overhead Considerations

The integration of the AI accelerator, configurable signal processing data path, and power management logic introduces a modest increase in silicon area compared to baseline architectures. However, this overhead is partially offset by the elimination of redundant processing units and the consolidation of on-chip memory resources. The resulting area-energy-performance trade-off is favorable for embedded applications, where the benefits of extended battery life, reduced thermal stress, and improved reliability outweigh modest area increases.

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V. Discussion and Future Directions

The experimental results confirm that holistic architectural integration—combining specialized acceleration, shared memory hierarchies, and adaptive power management—is essential for achieving energy efficiency in embedded AI systems. Several key observations emerge from this analysis:

First, the shared on-chip memory hierarchy plays a decisive role in mitigating the energy premium associated with off-chip memory accesses. This finding underscores the importance of memory-centric design approaches for data-intensive AI workloads.

Second, the heterogeneous response of power-saving techniques to different workload classes highlights the need for workload-aware optimization. AI-based image processing tasks benefit disproportionately from data reuse optimizations due to their higher computational density, while classical signal processing workloads are well-served by clock gating and reduced memory access overhead.

Third, the demonstrated energy proportionality suggests that adaptive power management can successfully navigate the trade-off between performance and energy consumption across varying workload intensities.

Future research directions include full ASIC implementation and silicon validation to confirm energy and area benefits under real operating conditions. Additional promising directions include the integration of reliability-aware techniques to address aging, soft errors, and process variation in scaled technologies; exploration of emerging non-volatile memory technologies for weight storage and in-memory computing; and extension of the architecture to support additional AI models beyond CNNs, including recurrent neural networks and transformers for sequential signal processing applications.

VI. Conclusion

This review has examined the design and implementation of low-power embedded VLSI architectures for AI-driven signal and image processing systems. The integrated architecture combining specialized AI acceleration, configurable signal processing data paths, shared on-chip memory hierarchies, and adaptive power management techniques offers a compelling solution to the energy efficiency challenges of edge AI deployment. Quantitative analysis demonstrates substantial power savings and improved energy proportionality compared to conventional embedded platforms, with modest area overhead. As AI capabilities continue to expand and power constraints tighten, such holistic architecture-algorithm co-design approaches will become increasingly essential for enabling intelligent edge computing applications.

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